
Software Programmable Adc And Dac Interfaces In Vhdl

14-bit, 4-channel, software-programmable, multiranging ... - the max1338 14-bit, analog-to-digital converter (adc) offers four simultaneously sampled, fully differential input channels, with independent track-and-hold (t/h) circuitry for each channel. the input channels are individually software programmable for input ranges of $\pm 10v$, $\pm 5v$, $\pm 2.5v$, and $\pm 1.25v$. the input channels feature fault tolerance ... **software programmable adc and dac interfaces in vhdl** - software programmable adc and dac interfaces in vhdl iosrjournals 13 | page is a disadvantage when the final system is uncertain or several peripherals with different characteristics need to **gain agility with the most programmable cloud-ready adc** - within each series through on-demand software licensing, which enables organizations to support growth without new hardware.

- operational scaling—virtualize adc services with a multi-tenant architecture that supports a variety of big-ip versions and product modules on a single device.

f5 virtual 16-bit, 750 ksps, unipolar/bipolar programmable input ... - 16-bit, 750 ksps, unipolar/bipolar programmable input pulsar® adc data sheet ad7612 rev. a document feedback information furnished by analog devices is believed to be accurate and reliable. **8-bit c microcontroller with 4/8k bytes in-system ...** - † a 6-channel, 10-bit adc - 8 in 32-lead tqfp, 32-pad qfn, and 32-ball ufbga packages † a programmable watchdog timer with internal oscillator † three software selectable power saving modes. the device includes the following modes for saving power: † idle mode: stops the cpu while allowing the timer/counter, adc, analog comparator, spi, **adc16 calibration procedure and programmable delay block ...** - adc16 calibration procedure and programmable delay block synchronization, rev. 1 adc16 calibration 2 freescale semiconductor trigger mode. this application note mainly describes how adc is used in energy metering application. **adc16 calibration procedure and programmable delay block ...** - adc16 calibration procedure and programmable delay block synchronization, rev. 1 adc16 and programmable delay block (pdb) integration 8 freescale semiconductor every adc has associated differential input, temperature sensor, bandgap, vrefo, and vrefl channels. **8-bit atmel microcontroller with 128kbytes in-system ...** - channel, 10-bit adc with optional differential input stage with programmable gain, programmable watchdog timer with internal oscillator, an spi serial port, ieee std. 1149.1 compliant jtag test interface, also used for accessing the on-chip debug system and programming and six software selectable power saving modes. **ads868x 16-bit, high-speed, single-supply, sar adc data ...** - adc driver v bias ain_p ain_gnd 4.096-v reference agnd dgnd refgnd avdd dvdd digital logic and interface refio refcap sclk sdi sdo 16-bit sar adc ads868x product folder order now technical documents tools & software support & community reference design an important notice at the end of this data sheet addresses availability, warranty, changes ... **integrated software-defined radio on zynq 7000 all ...** - integrated software-defined radio on zynq ®-7000 all programmable soc design seminar. 3 course objectives during this seminar, you will gain insight into avnet zynq-7000 ap soc / ad9361 software-defined radio kits ... o analog-to-digital converter inputs page 15 **adc with microphone input and programmable digital filters** - - programmable preamp gain - pseudo differential inputs with common mode rejection - programmable alc / noise gate in adc path • low-noise bias supplied for electret microphones other features • 5 band eq • programmable high pass filter (wind noise reduction) • fully programmable iir filter (notch filter) • on-chip pll **psoc® 4: psoc 4100s datasheet programmable system-on-chip ...** - programmable analog two opamps with reconfigurable high-drive external and high-bandwidth internal drive and comparator modes and adc input buffering capability. opamps can operate in deep sleep low-power mode. 12-bit 1-msps sar adc with differential and single-ended modes, and channel sequencer with signal averaging **12-bit, 4/8 channel, integrated analog input module for ...** - the analog input module reference design is intended as an evaluation module for users to develop end-equipment like plc, data acquisition, test and measurement systems etc. **rad-hard programmable sige adc, 3 gs/s at 12-bit, 500 ms/s ...** - rad-hard programmable sige adc, 3 gs/s at 12-bit, 500 ms/s at 14-bit resolution ridgetop's radiation-hardened programmable sige analog-to-digital data converter (adc) has fast digitization with extremely high ... software-defined radio telecommunications receivers automatic test equipment ip sub-blocks available with **rf-sampling adcs for software-defined radio** - software-defined radio platforms have programmable hardware and software, so a basic sdr architecture can be straightforward, pairing flexible software with a receiver consisting primarily of a low-noise amplifier, a filter, and the adc. the amplified rf signal is digitized directly without the need for downconversion, a local oscillator,

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